WEST Search History

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DATE: Tuesday, May 10, 2005

Hide?	Set Name	Query	Hit Count
	DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ		
☐	L21	(memory and head and tail).ti.	18
☐	L20	L19 and (head near5 pointer$1)	13
☐	L19	L18 and (tail near5 pointer$1)	13
☐	L18	L17 and (memory same cache)	28
☐	L17	L16 and (empty near5 queue)	28
☐	L16	L15 and queue	31
☐	L15	L14 and dequeue	31
☐	L14	L13 and (head near5 tail)	31
☐	L13	L12 and cache	38
☐	L12	L11 and descriptor	47
☐	L11	L10 and (queue same dequeue)	90
☐	L10	L9 and (head near5 point$2)	1281
☐	L9	(memory near5 structure)	76263
☐	L8	5671446 .uref.	13
☐	L7	(memory near5 head) same (queue near5 enqueue)	10
☐	L6	L3 and (head near5 point$)	10
☐	L5	L3 and (dequeue$1)	2
☐	L4	L3 and (dequeue near5 command$1)	0
☐	L3	(data and memory and queue$).ti.	280
☐	L2	'memory queue'.ti.	32
☐	L1	'memory enqueue'.ti.	0

END OF SEARCH HISTORY

Hit List

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Search Results - Record(s) 1 through 32 of 32 returned.

☐ 1. Document ID: US 20020116538 A1

Using default format because multiple data bases are involved.

L2: Entry 1 of 32 File: PGPB Aug 22, 2002

PGPUB-DOCUMENT-NUMBER: 20020116538
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020116538 A1

TITLE: High-performance memory queue

PUBLICATION-DATE: August 22, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Chen, Shawfu	New Milford	CT	US	
Dryfoos, Robert O.	Hopewell Junction	NY	US	
Feldman, Allan	Poughkeepsie	NY	US	
Hu, David Y.	Poughkeepsie	NY	US	
Keenaghan, Jason A.	Wappingers Falls	NY	US	
Sutton, Peter G.	Lagrangeville	NY	US	
Wang, Mei-Hui	Brookfield	CT	US	

US-CL-CURRENT: 719/314; 718/101, 718/104

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 6157963 A

L2: Entry 2 of 32 File: USPT Dec 5, 2000

US-PAT-NO: 6157963
DOCUMENT-IDENTIFIER: US 6157963 A

TITLE: System controller with plurality of memory queues for prioritized scheduling of I/O requests from priority assigned clients

DATE-ISSUED: December 5, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Courtright, II; William V.	Wichita	KS		

Delaney; William P.	Wichita	KS
Fredin; Gerald J.	Wichita	KS

US-CL-CURRENT: 710/5; 710/40

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

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☐ 3. Document ID: US 6137807 A

L2: Entry 3 of 32 File: USPT Oct 24, 2000

US-PAT-NO: 6137807
DOCUMENT-IDENTIFIER: US 6137807 A

TITLE: Dual bank queue memory and queue control system

DATE-ISSUED: October 24, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rusu; Marinica	Sunnyvale	CA		
Jaser; Ihab A.	San Jose	CA		

US-CL-CURRENT: 370/429; 370/412, 370/422, 710/52

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

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☐ 4. Document ID: US 5832304 A

L2: Entry 4 of 32 File: USPT Nov 3, 1998

US-PAT-NO: 5832304
DOCUMENT-IDENTIFIER: US 5832304 A

TITLE: Memory queue with adjustable priority and conflict detection

DATE-ISSUED: November 3, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Bauman; Mitchell A.	Circle Pines	MN		
Carlin; Jerome G.	Shoreview	MN		
Gilbertson; Roger L.	Minneapolis	MN		

US-CL-CURRENT: 710/40; 710/39, 711/151, 711/158

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

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☐ 5. Document ID: NA9406319

L2: Entry 5 of 32 File: TDBD Jun 1, 1994

TDB-ACC-NO: NA9406319

DISCLOSURE TITLE: Memory Queue Priority Mechanism for a RISC Processor

PUBLICATION-DATA:
IBM Technical Disclosure Bulletin, June 1994, US

VOLUME NUMBER: 37
ISSUE NUMBER: 6A
PAGE NUMBER: 319 - 322

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 6. Document ID: NN9208382

L2: Entry 6 of 32 File: TDBD Aug 1, 1992

TDB-ACC-NO: NN9208382

DISCLOSURE TITLE: Blocked Data Transfer with Virtual Memory Queues.

PUBLICATION-DATA:
IBM Technical Disclosure Bulletin, August 1992, US

VOLUME NUMBER: 35
ISSUE NUMBER: 3
PAGE NUMBER: 382 - 385

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 7. Document ID: US 6813249 B1

L2: Entry 7 of 32 File: DWPI Nov 2, 2004

DERWENT-ACC-NO: 2004-819710

DERWENT-WEEK: 200481
COPYRIGHT 2005 DERWENT INFORMATION LTD
TITLE: Network based data cells prefetching system in data communication system, has memory controller to prefetch data cells from host that are associated with assigned address, and prefetched cells are stored in selected memory queues

INVENTOR: FOSMARK, K S; LAUFFENBURGER, K A ; PERRY, W A ; SHELOR, C F ; WHALEY, A

PRIORITY-DATA: 1999US-0251110 (February 16, 1999)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 6813249 B1	November 2, 2004		013	H04L012/28

INT-CL (IPC): G01 R 31/08; G06 F 11/00; G08 C 15/00; H04 J 1/16; H04 J 3/14; H04 L 12/28; H04 L 12/56

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 8. Document ID: JP 2004320459 A

L2: Entry 8 of 32 File: DWPI Nov 11, 2004

DERWENT-ACC-NO: 2004-808379
DERWENT-WEEK: 200480
COPYRIGHT 2005 DERWENT INFORMATION LTD
TITLE: Output band estimation method for packet network, involves measuring queue length of packet collected in waiting buffer for every preset measuring period, and storing it in memory for queue length distribution determination

PRIORITY-DATA: 2003JP-0111731 (April 16, 2003)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 2004320459 A	November 11, 2004		015	H04L012/56

INT-CL (IPC): H04 L 12/56

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 9. Document ID: KR 2004065585 A

L2: Entry 9 of 32 File: DWPI Jul 23, 2004

DERWENT-ACC-NO: 2004-773331
DERWENT-WEEK: 200476
COPYRIGHT 2005 DERWENT INFORMATION LTD
TITLE: Fast mail forwarding system using memory queue

INVENTOR: KIM, Y S

PRIORITY-DATA: 2003KR-0002584 (January 15, 2003)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
KR 2004065585 A	July 23, 2004		001	G06F017/60

INT-CL (IPC): G06 F 17/60

☐ 10. Document ID: WO 2004077221 A2

L2: Entry 10 of 32 File: DWPI Sep 10, 2004

DERWENT-ACC-NO: 2004-662124
DERWENT-WEEK: 200464
COPYRIGHT 2005 DERWENT INFORMATION LTD
TITLE: Network resource management system for computer system, maps network data and stores mapped data in memory in queue format, and transmits responses with respect to requests received from client terminal

INVENTOR: RAO, V K

PRIORITY-DATA: 2003IN-MU00127 (January 30, 2003)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
WO 2004077221 A2	September 10, 2004	E	020	G06F000/00

INT-CL (IPC): G06 F 0/00

☐ 11. Document ID: US 20040151191 A1

L2: Entry 11 of 32 File: DWPI Aug 5, 2004

DERWENT-ACC-NO: 2004-614156
DERWENT-WEEK: 200459
COPYRIGHT 2005 DERWENT INFORMATION LTD
TITLE: Data frame processing apparatus for use in networking device e.g. protocol bridge, has embedded processors to copy header of fibre channel frame entry to other entry of memory queues and to encapsulate frame in another frame

INVENTOR: FUREY, S; GEDDES, D ; MORETTI, M ; SURI, S ; WU, T

PRIORITY-DATA: 2003US-441764P (January 21, 2003), 2003US-0445105 (May 23, 2003)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 20040151191 A1	August 5, 2004		018	H04L012/28

INT-CL (IPC): G06 F 15/16; H04 L 12/28; H04 L 12/56

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 12. Document ID: US 20040131068 A1, EP 1432179 A1

L2: Entry 12 of 32 File: DWPI Jul 8, 2004

DERWENT-ACC-NO: 2004-490045
DERWENT-WEEK: 200447
COPYRIGHT 2005 DERWENT INFORMATION LTD
TITLE: Multi-channel network node, has memory unit organized as physical memory queues with coherent memory and switching unit routes data from input port to memory queue that is assigned to destined output port

INVENTOR: DEMBECK, L; KOERBER, W ; KORBER, W

PRIORITY-DATA: 2002EP-0360348 (December 16, 2002)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 20040131068 A1	July 8, 2004		000	H04L012/28
EP 1432179 A1	June 23, 2004	E	010	H04L012/56

INT-CL (IPC): H04 L 12/28; H04 L 12/56

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 13. Document ID: US 20040143829 A1, JP 2004151761 A

L2: Entry 13 of 32 File: DWPI Jul 22, 2004

DERWENT-ACC-NO: 2004-434902
DERWENT-WEEK: 200449
COPYRIGHT 2005 DERWENT INFORMATION LTD
TITLE: Memory controller in computer system, changes data stored in shared memory, when cache memory processor executes command stored in shared memory queue

INVENTOR: KUWABARA, H; MITSUOKA, Y ; UCHIUMI, K

PRIORITY-DATA: 2002JP-0313027 (October 28, 2002)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 20040143829 A1	July 22, 2004		000	G06F012/00
JP 2004151761 A	May 27, 2004		013	G06F011/00

INT-CL (IPC): G06 F 9/44; G06 F 11/00; G06 F 12/00

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 14. Document ID: US 20030236946 A1

L2: Entry 14 of 32 File: DWPI Dec 25, 2003

DERWENT-ACC-NO: 2004-107505
DERWENT-WEEK: 200411
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TITLE: Memory queue management process for computer system, involves dividing memory address space into multiple buffers and associating header cells that indicate unique memory address of buffer, to buffers

INVENTOR: GREUBEL, J D

PRIORITY-DATA: 2002US-0176362 (June 20, 2002)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 20030236946 A1	December 25, 2003		009	G06F012/00

INT-CL (IPC): G06 F 12/00

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

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☐ 15. Document ID: JP 2003263883 A, US 20030172242 A1

L2: Entry 15 of 32 File: DWPI Sep 19, 2003

DERWENT-ACC-NO: 2003-766517
DERWENT-WEEK: 200372
COPYRIGHT 2005 DERWENT INFORMATION LTD
TITLE: Self synchronous first-in and first-out memory for use as queue buffer, adjusts timing of write/read request signal from external devices, and calculates write/read addresses based on request signals

INVENTOR: ONOZAKI, M; UNEYAMA, T

PRIORITY-DATA: 2002JP-0062107 (March 7, 2002)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 2003263883 A	September 19, 2003		020	G11C007/00
US 20030172242 A1	September 11, 2003		034	G06F012/00

INT-CL (IPC): G06 F 12/00; G06 F 13/38; G11 C 7/00

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

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☐ 16. Document ID: US 6463059 B1

L2: Entry 16 of 32 File: DWPI Oct 8, 2002

DERWENT-ACC-NO: 2003-110250
DERWENT-WEEK: 200310
COPYRIGHT 2005 DERWENT INFORMATION LTD
TITLE: Digital transport packet distribution management method in digital multimedia communication system, involves adding local header incorporating memory queue address index to each transport packet

INVENTOR: HOEM, R H; LAI, B ; MOVSHOVICH, A ; PUTTASWAMY, N A

PRIORITY-DATA: 1998US-0205480 (December 4, 1998)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 6463059 B1	October 8, 2002		024	H04L012/56

INT-CL (IPC): H04 L 12/54; H04 L 12/56

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 17. Document ID: US 6829769 B2, US 20020144006 A1

L2: Entry 17 of 32 File: DWPI Dec 7, 2004

DERWENT-ACC-NO: 2003-091485
DERWENT-WEEK: 200480
COPYRIGHT 2005 DERWENT INFORMATION LTD
TITLE: Interprocess communication method involves accessing shared memory heaps to place instruction in allocated memory region, and to add agnostic memory handle to memory queues

INVENTOR: CRANSTON, W M; PURTELL, M J ; YANG, M

PRIORITY-DATA: 2000US-238106P (October 4, 2000), 2001US-0823124 (March 30, 2001)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 6829769 B2	December 7, 2004		000	G06F009/46
US 20020144006 A1	October 3, 2002		021	G06F009/46

INT-CL (IPC): G06 F 9/00; G06 F 9/46; G06 F 9/54; G06 F 15/163

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 18. Document ID: US 20020115428 A1

L2: Entry 18 of 32 File: DWPI Aug 22, 2002

DERWENT-ACC-NO: 2002-749901
DERWENT-WEEK: 200281
COPYRIGHT 2005 DERWENT INFORMATION LTD
TITLE: Wireless data retrieval device for personal digital assistant, has FIFO memory queue which stores standardized correspondence information for being

transmitted to and received from wireless channel

INVENTOR: STORINO, S N; UHLMANN, G J

PRIORITY-DATA: 2001US-0789283 (February 20, 2001)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 20020115428 A1	August 22, 2002		008	H04M011/10

INT-CL (IPC): H04 M 11/10

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

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☐ 19. Document ID: US 20020112105 A1

L2: Entry 19 of 32 File: DWPI Aug 15, 2002

DERWENT-ACC-NO: 2003-016373
DERWENT-WEEK: 200301
COPYRIGHT 2005 DERWENT INFORMATION LTD
TITLE: Computer system for service aware network, has circular memory queue defined between designated addresses in local memory of receiving CPU

INVENTOR: DANIEL, M; ZEIRA, A

PRIORITY-DATA: 2001US-0782090 (February 12, 2001)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 20020112105 A1	August 15, 2002		011	G06F003/00

INT-CL (IPC): G06 F 3/00

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

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☐ 20. Document ID: US 6055598 A

L2: Entry 20 of 32 File: DWPI Apr 25, 2000

DERWENT-ACC-NO: 2000-364194
DERWENT-WEEK: 200031
COPYRIGHT 2005 DERWENT INFORMATION LTD
TITLE: Bus-to-bus bridging architecture has FIFO memory queues which are arranged to store commands in specific sequence

INVENTOR: LANGE, R E

PRIORITY-DATA: 1996US-0718971 (September 26, 1996)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 6055598 A	April 25, 2000		018	G06F013/38

INT-CL (IPC): G06 F 13/38

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 21. Document ID: JP 11249962 A

L2: Entry 21 of 32 File: DWPI Sep 17, 1999

DERWENT-ACC-NO: 1999-575813
DERWENT-WEEK: 199949
COPYRIGHT 2005 DERWENT INFORMATION LTD
TITLE: Disc subsystem with cache memory, for computer system - performs transition of updating data of low probability hit to higher-order instruction by cache re-assignment possible queue after finishing write-in to disc apparatus, when managing cache memory by queues

PRIORITY-DATA: 1998JP-0053103 (March 5, 1998)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 11249962 A	September 17, 1999		004	G06F012/08

INT-CL (IPC): G06 F 12/08; G06 F 12/12

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 22. Document ID: US 5848234 A

L2: Entry 22 of 32 File: DWPI Dec 8, 1998

DERWENT-ACC-NO: 1999-059542
DERWENT-WEEK: 199905
COPYRIGHT 2005 DERWENT INFORMATION LTD
TITLE: Object procedure messaging method in computer network - involves determining whether selected server is on first platform, based on which network transport or memory queue are selected for communication between client and server

INVENTOR: CHERNICK, A; GREENBLATT, S ; LACKEY, R L ; NEELEY, W K ; YANG, D

PRIORITY-DATA: 1994US-0247178 (May 20, 1994), 1993US-0065926 (May 21, 1993), 1996US-0653106 (May 24, 1996)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 5848234 A	December 8, 1998		015	G06F015/16

INT-CL (IPC): G06 F 15/16

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 23. Document ID: JP 10254966 A

L2: Entry 23 of 32 File: DWPI Sep 25, 1998

DERWENT-ACC-NO: 1998-573303
DERWENT-WEEK: 199849
COPYRIGHT 2005 DERWENT INFORMATION LTD
TITLE: Information presentation system connected to Internet - has display controller which displays advertisement data stored in memory when queue of contents is formed while acquiring contents from network

PRIORITY-DATA: 1997JP-0061567 (March 14, 1997)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 10254966 A	September 25, 1998		008	G06F017/60

INT-CL (IPC): G06 F 13/00; G06 F 17/60; G09 G 5/00

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 24. Document ID: EP 745938 A1, JP 08328944 A

L2: Entry 24 of 32 File: DWPI Dec 4, 1996

DERWENT-ACC-NO: 1997-013900
DERWENT-WEEK: 199709
COPYRIGHT 2005 DERWENT INFORMATION LTD
TITLE: Main storage unit with operating system resource region and user region - has user region memories designated by full address to access any main storage areas, memories form queue, several pointers in OS resource region each store full address, OS resource headers pointers indicate next memory in queue

INVENTOR: NAKAJIMA, T

PRIORITY-DATA: 1995JP-0133969 (May 31, 1995)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
EP 745938 A1	December 4, 1996	E	011	G06F012/02
JP 08328944 A	December 13, 1996		009	G06F012/02

INT-CL (IPC): G06 F 12/02

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 25. Document ID: EP 725345 A1, US 6393503 B2, CA 2167632 A, JP 10307732 A, US

20010023467 A1

L2: Entry 25 of 32 File: DWPI Aug 7, 1996

DERWENT-ACC-NO: 1996-356257
DERWENT-WEEK: 200239
COPYRIGHT 2005 DERWENT INFORMATION LTD
TITLE: Inter process communication method using shared memory - involves creating shared memory queue and passing pointer to consuming process to remove message from queue

INVENTOR: CLARK, T M; FISHLER, L R

PRIORITY-DATA: 1995US-0377303 (January 23, 1995), 2001US-0867783 (May 29, 2001)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
EP 725345 A1	August 7, 1996	E	073	G06F011/14
US 6393503 B2	May 21, 2002		000	G06F013/00
CA 2167632 A	July 24, 1996		000	G06F015/163
JP 10307732 A	November 17, 1998		015	G06F009/46
US 20010023467 A1	September 20, 2001		000	G06F013/38

INT-CL (IPC): G06 F 9/46; G06 F 11/14; G06 F 13/00; G06 F 13/38; G06 F 13/40; G06 F 15/163

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 26. Document ID: US 5442747 A

L2: Entry 26 of 32 File: DWPI Aug 15, 1995

DERWENT-ACC-NO: 1995-292801
DERWENT-WEEK: 199538
COPYRIGHT 2005 DERWENT INFORMATION LTD
TITLE: Flexible multiport multi-format burst buffer for multimedia video chip - uses single cache memory to queue number of asynchronous data streams to be stored and retrieved from DRAM

INVENTOR: CHAN, S S; KIMURA, S A ; SIMPSON, M S

PRIORITY-DATA: 1993US-0127219 (September 27, 1993)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 5442747 A	August 15, 1995		012	G06F012/00

INT-CL (IPC): G06 F 12/00

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 27. Document ID: US 6718399 B1, WO 9428486 A1, AU 9469577 A

L2: Entry 27 of 32 File: DWPI Apr 6, 2004

DERWENT-ACC-NO: 1995-023070
DERWENT-WEEK: 200425
COPYRIGHT 2005 DERWENT INFORMATION LTD
TITLE: Communication between client and server objects - involves using network transport between operating platforms or using memory queue on platforms to communicate between client and server object

INVENTOR: CHERNICK, A; GREENBLATT, S ; LACKEY, R L ; NEELEY, W K ; YANG, D

PRIORITY-DATA: 1993US-0065926 (May 21, 1993), 1995US-0432372 (May 1, 1995), 1996US-0660730 (June 10, 1996)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 6718399 B1	April 6, 2004		000	G06F009/46
WO 9428486 A1	December 8, 1994	E	045	G06F013/00
AU 9469577 A	December 20, 1994		000	G06F013/00

INT-CL (IPC): G06F 9/46; G06F 13/00

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw. D

☐ 28. Document ID: EP 609051 A1, US 5848283 A

L2: Entry 28 of 32 File: DWPI Aug 3, 1994

DERWENT-ACC-NO: 1994-242389
DERWENT-WEEK: 199905
COPYRIGHT 2005 DERWENT INFORMATION LTD
TITLE: Maintaining data coherency among main and cache memories using cache synchronisation - establishing multi-state bus synchronisation flag and issuing bus operation request to memory queue and thereafter to common bus

INVENTOR: MOORE, C R; MUHICH, J S ; VICKNAIR, B J

PRIORITY-DATA: 1993US-0010900 (January 29, 1993)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
EP 609051 A1	August 3, 1994	E	015	G06F012/08
US 5848283 A	December 8, 1998		000	G06F013/00

INT-CL (IPC): G06F 12/08; G06F 13/00

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw. D

☐ 29. Document ID: US 5319753 A

L2: Entry 29 of 32 File: DWPI Jun 7, 1994

DERWENT-ACC-NO: 1994-182968
DERWENT-WEEK: 199422
COPYRIGHT 2005 DERWENT INFORMATION LTD
TITLE: Bidirectional interrupt appts - handles programmable length interrupt messages between two devices, e.g. two processors, through dual, programmably defined memory queues

INVENTOR: MACKENNA, C A; NIMISHAKAVI, H ; SWAMI, R

PRIORITY-DATA: 1992US-0953732 (September 29, 1992)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 5319753 A	June 7, 1994		012	G06F013/24

INT-CL (IPC): G06F 13/24

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 30. Document ID: KR 9403300 B1

L2: Entry 30 of 32 File: DWPI Apr 20, 1994

DERWENT-ACC-NO: 1996-048030
DERWENT-WEEK: 199605
COPYRIGHT 2005 DERWENT INFORMATION LTD
TITLE: Memory queue for pipeline bus protocol system - includes buffer for storing continuous transmission requests from system bus when memory controller cannot process any more request until previous request have been executed

INVENTOR: KIM, A; PARK, B ; SHIM, W ; YUN, Y

PRIORITY-DATA: 1991KR-0019573 (November 5, 1991)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
KR 9403300 B1	April 20, 1994		000	G06F013/42

INT-CL (IPC): G06F 13/42

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 31. Document ID: EP 239097 A, DE 3750702 G, EP 239097 B1, US 4847748 A

L2: Entry 31 of 32 File: DWPI Sep 30, 1987

DERWENT-ACC-NO: 1987-272560
DERWENT-WEEK: 198739
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TITLE: Data processing system with decoded instruction queue memory - has queue structure composed of entries for latching entry information and including up=down counter

INVENTOR: SATO, Y; YAMAHATA, H

PRIORITY-DATA: 1986JP-0067843 (March 25, 1986)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
EP 239097 A	September 30, 1987	E	043	
DE 3750702 G	December 8, 1994		000	G06F009/38
EP 239097 B1	November 2, 1994	E	023	G06F009/38
US 4847748 A	July 11, 1989		020	

INT-CL (IPC): G06F 9/38

☐ 32. Document ID: US 3979733 A, BE 841524 A, CA 1056065 A, DE 2620220 A, DE 2620220 B, FR 2310595 A, GB 1497002 A, IT 1062464 B, NL 180371 B, NL 7604729 A, SE 7605192 A

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Search Results - Record(s) 1 through 2 of 2 returned.

☐ 1. Document ID: US 6393531 B1

Using default format because multiple data bases are involved.

L5: Entry 1 of 2 File: USPT May 21, 2002

US-PAT-NO: 6393531
DOCUMENT-IDENTIFIER: US 6393531 B1
**** See image for Certificate of Correction ****

TITLE: Queue based data control mechanism for queue based memory controller

DATE-ISSUED: May 21, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Novak; Stephen T.	South Lake Tahoe	CA		
Peck, Jr.; John C.	Mountain View	CA		

US-CL-CURRENT: 711/154; 365/189.12, 711/109, 711/159, 711/165, 713/600

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 2. Document ID: US 20050055534 A1

L5: Entry 2 of 2 File: DWPI Mar 10, 2005

DERWENT-ACC-NO: 2005-232052
DERWENT-WEEK: 200524
COPYRIGHT 2005 DERWENT INFORMATION LTD
TITLE: Data processing system executes instruction to transfer data stream between memory and general purpose register, and to be queued in memory or register, and instruction comprising source operand to selectively dequeue data stream

INVENTOR: MOYER, W C

PRIORITY-DATA: 2003US-0657593 (September 8, 2003)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 20050055534 A1	March 10, 2005		026	G06F015/00

INT-CL (IPC): G06 F 15/00

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IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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1. **Priority queues and sorting methods for parallel simulation**
Grammatikakis, M.D.; Liesche, S.;
Software Engineering, IEEE Transactions on
Volume 26, Issue 5, May 2000 Page(s):401 - 422
AbstractPlus | References | Full Text: PDF(5408 KB) IEEE JNL

2. **An O(log/sup 2/ N) parallel algorithm for output queuing**
Prakash, A.; Sharif, S.; Aziz, A.;
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3. **Reducing run queue contention in shared memory multiprocessors**
Dandamudi, S.P.;
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Volume 30, Issue 3, March 1997 Page(s):82 - 89
AbstractPlus | References | Full Text: PDF(152 KB) IEEE JNL

4. **Memory ordering: a value-based approach**
Cain, H.W.; Lipasti, M.H.;
Computer Architecture, 2004. Proceedings. 31st Annual International Symposium on
19-23 June 2004 Page(s):90 - 101
AbstractPlus | Full Text: PDF(387 KB) IEEE CNF

5. **Design of virtual channel queue in an ATM broadband terminal adaptor**
Chao, H.J.; Smith, D.E.;
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4-8 May 1992 Page(s):294 - 302 vol.1
AbstractPlus | Full Text: PDF(520 KB) IEEE CNF

6. **Queuing spin lock algorithms to support timing predictability**
Craig, T.S.;
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AbstractPlus | Full Text: PDF(716 KB) IEEE CNF

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7-11 March 2005 Page(s):112 - 117 Vol. 3
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Exercises 6: Linked-List **Queue** Management (U.Crete, CS-534)
... all **head pointers** (Hd) of all **queues**, all **tail pointers** (Tl) of all **queues**,
... of **descriptors** that is twice the number of buffer **memory** segments. ...
archvlsi.ics.forth.gr/~kateveni/534/03a/ex06_ll_mgt.htm - 10k - Cached - Similar pages

Exercises 5: Multi-Packet Blocks, Multicast **Queues** (U.Crete, CS-534)
... The **head** and **tail pointers** of each **queue**, on the other hand, ... to have a number of **descriptors** that is twice the number of buffer **memory** segments. ...
archvlsi.ics.forth.gr/~kateveni/534/05a/ex05_advq.html - 10k - Cached - Similar pages

The Next Generation of Intel IXP Network Processors
... Locating the data store for the cache of **queue descriptors** at the **memory** controller ... and these reference 1 of 16 data store **tail** or **head pointers**. ...
www.intel.com/technology/itj/2002/ volume06issue03/art01_nextgenixp/p09_challenges.htm - 52k - Cached - Similar pages

The Next Generation of Intel IXP Network Processors
... tends to have many small data structures such as **queue descriptors** and linked lists. ... The SRAM controller keeps the **head** and **tail pointers** in on-chip ...
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[PDF] Using the RapidIO Messaging Unit on PowerQUICC III
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... In chaining mode, the software must reserve an area of **memory** to store message **descriptors**. ... /*set up the **head** and **tail pointers** for the **queue**. */ ...
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[PDF] A Fully-Programmable **Memory** Management System Optimizing **Queue** ...
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... Categories and Subject **Descriptors**. B.3 **Memory** Structures, B.6 Logic Design
... **Head Tail. Head Tail**. E. 1. 0. 1. 1. E. 0. **Queue** Table. Packet. **pointers** ...
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... in the **memory** management mechanism and the associated non blocking **queue** ...
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File Format: PDF/Adobe Acrobat - View as HTML
... consisting of **head** and **tail. pointers** and the **queue** length, and the linked lists
... b) **queue descriptors** are stored in external **memory** and ...
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EPICURE Design Note 6.3<P> <b> Use of the QVI and Common VME ...
... of scalar items and CM-relative **pointers** (offsets relative to the CM base,
... The **tail pointer** is the CM-**pointer** to the last (**tail**) entry on the **queue** ...

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[PPT] Design and Simulation of IRAM Network Interface
File Format: Microsoft Powerpoint 97 - View as HTML
... Manages multiple FIFO **queues** in one shared **memory**. 5 **queues**: ... Each **queue** is represented as a linked list with **head/tail**/next **pointers** ...
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... **memory**, program global variables. signal actions, message **queues**, timers ...
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... described in Work **Queue** Requests (WQR), or **descriptors**, ... spective **head pointers** and **tail pointers**. The buffers run out ...
www.osc.edu/~pw/papers/liu-mpi-ib-ics03.pdf - Similar pages

Patent 5089958: Fault tolerant computer backup system
... The **queue** is arranged in a circular fashion, with **head** and **tail pointers** ... with the **tail pointer** for the **queue**, which is contained in clock RAM, ...
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Patent 5848068: ATM communication system interconnect/termination unit
... **pointers** to the **head** end of a linked list of Virtual Circuit **Descriptors** ... has a **head** and a **tail pointer** with four bytes for each, the total **memory** ...
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RVM: Recoverable Virtual **Memory**, Release 1.3: RVM Internals
... If truncation is not in progress, both of the **pointers** prev_log_head and ... a lot of disk **head** seeks between the log status block and the log **tail**, ...
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ABSTRACT

Shared-memory provides a uniform and attractive mechanism for communication. For efficiency, it is often implemented with a layer of interpretive hardware on top of a message-passing communications network. This interpretive layer is responsible for data location, data movement, and cache coherence. It uses patterns of communication that benefit common programming styles, but which are only heuristics. This suggests that certain styles of communication may benefit from direct access to the underlying communications substrate. The Alewife machine, a shared-memory multiprocessor being built at MIT, provides such an interface. The interface is an integral part of the shared memory implementation and affords direct, user-level access to the network queues, supports an efficient DMA mechanism, and includes fast trap handling for message reception. This paper discusses the design and implementation of the Alewife message-passing interface and addresses the issues and advantages of using such an interface to complement hardware-synthesized shared memory.

REFERENCES

Note: OCR errors may be found in this Reference List extracted from the full text article. ACM has opted to expose the complete List rather than only correct and linked references.

1 A. Agarwal , D. Chaiken , K. Johnson , D. Kranz , J. Kubiatowicz , K. Kurihara , B. H. Lim , G. Maa , D. Nussbaum , M. Parkin , D. Yeung, THE MIT ALEWIFE MACHINE: A LARGE-SCALE DISTRIBUTED-MEMORY MULTIPROCESSOR, Massachusetts Institute of Technology, Cambridge, MA,

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Autonomous Maneuvers of a Nonholonomic Vehicle - Paromtchik, Garnier, Laugier (1997) (Correct)
angle and locomotion velocity are two control **commands** (OE v)Equations (1) correspond to a system
ftp.inrialpes.fr/pub/INRIA/projets/SHARP/publications/paromtchik:etat:iser:97.ps.gz

WAMM (Wide Area Metacomputer Manager): User's Guide - Version Ranieri (Correct)
PVMTasker: used by wamm to execute remote **commands** and to receive information on PVM tasks running
www.hensa.ac.uk/parallel/environments/pvm3/wamm/ug-eng.ps.gz

A Layered Approach for an Autonomous Robotic Soccer System - Veloso, Stone, Achim (1997) (Correct)
what to do next the client selects navigational **commands** to send to its corresponding robot agent these
is also provided with a probabilistic predictive **memory** to account for the inaccessibility of the
www.cs.cmu.edu/afs/cs/user/mmv/www/papers/soccer:agents.ps.gz

A Reactive Constraint Logic Programming Scheme - Fages, Fowler, Sola (1995) (Correct) (5 citations)
to consider external events as query modification **commands**. Maher and Stuckey [11] defined an incremental
www.dmi.ens.fr/~fages/Papers/iclp95.ps.gz

Parallel Database Management System: Kappa - Kawamura, KAWAMURA (1994) (Correct) (2 citations)
Kappa-P has two kinds of operations: primitive **commands** and a query language based on extended
will require more processing power and secondary **memory** to manage it. Such situations requires a parallel
www.icot.or.jp/AITEC/PUB/FGCS-Proc/PS/kappa.ps.gz

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to collect all the observed data with the motor **commands** taken during the observation and to estimate the
that I is as small as possible with respect to the **memory** size. For n, complex behaviors of other agents
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physical robotic effectors execute the motion **commands** generated by the cognition level. In this paper,
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The Hippocampus And Cerebellum In Adaptively Timed.. - Grossberg, Merrill (1995) (Correct) (3 citations)
to salient cues could prematurely release motor **commands** were not the release of these **commands**
manuscript. ABSTRACT The concepts of declarative **memory** and procedural **memory** have been used to
cns-ftp.bu.edu/pub/diana/GroMer96.ps.gz

Experiences With an Environment Generation System - Popovich, Schell, Perry (Correct)
that occur as side effects of normal editing **commands**, and extended **commands**, which, true to their
www.bell-labs.com/~dep/work/papers/icse13.ps.gz

System Monitor for Network of Workstations - Isaac Cheng (Correct)
data, we wrote a Perl script that runs system **commands** on each of the machines in NOW. To collect load
the number and speeds of processors, amount of **memory**, devices, operating system versions and patches,
http.cs.berkeley.edu/~isaacc/projects/262r.ps.gz

North American ISDN Users' Forum Application Software Interface .. - Part Ms-Dos (Correct)
study. Note: The PE's callback routine should only **queue** messages and return immediately so that the
6.0. ARDD **Commands**
error 0x82 Invalid message pointer 0x83 Out of **memory** 0x84 Function not supported 0x85 Interface Busy
isdn.ncsl.nist.gov/niuf/404-92-2.ps

Hybrid Dynamical Systems - Göllü, Varaiya (1993) (Correct) (25 citations)
At the upper layer the supervisor issues symbolic **commands**. Some time after a **command** is issued the the read/write head system is better modeled as a **memory**less logic function which accepts a read or write
www-path.eecs.berkeley.edu/~gollu/Papers/hds.ps

Isabelle Tutorial and User's Manual - Paulson, Nipkow (1990) (Correct) (21 citations)
: 13 1.3.1 Basic **commands** :
turing.wins.uva.nl/~mdr/ACLG/Provers/Isabelle/Papers/ROOT.ps.gz

Mars Pathfinder Microrover - Implementing A Low Cost Planetary.. - J.Matijevic (Correct) (4 citations)
to avoid obstacles but continues to achieve the **commanded** goal location 7 .While the vehicle is
protocol, **command** and telemetry formats, and the **memory** management and processing architecture of the
mpfwww.jpl.nasa.gov/roverctrlnav/IAA96_jake.ps

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and assumes that you are executing it as the first **command** after you load in our packages. Single-letter
www.math.washington.edu/~vityaev/algdemo.ps

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for a client are turn, dash, kick and say. The say **command** cause the simulator to send an auditory message
Predictive **Memory** for an Inaccessible Environment Mike Bowling
www.cs.cmu.edu/afs/cs/user/mmv/www/papers/IROS96b.ps.gz

Tcl/Tk for a Personal Digital Assistant - Karin Petersen (Correct)
Network Application Tcl GUI Tcl Interpreter Tcl **Commands** PDA Workstation Figure 1: Tcl as the link
other PDAs. A different approach was used for the **memory** prosthesis project at EuroPARC [LBC 94]in
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interacts with a software environment by issuing **commands** and interpreting the environment's feedback. A
execution. The agent has a limited episodic **memory**, and using this, is able to answer questions
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incremental actions and replacement of complex **command**-language syntax by direct manipulation of the
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The Safety Guaranteeing System at Station Hoorn-Kersenboogerd - Groote, van Vlijmen, Koorn (1995) (Correct) (27 citations)
movement. And a bottom layer which checks whether **commands** issued by the top layer can safely be executed
implementing the tool. But, due to the enormous **memory** consumption of this code, this route turned out
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RSIM: An Execution-Driven Simulator for ILP-Based Shared-Memory.. - Vijay Pai (1997) (Correct) (27 citations)

FPU Instruction Fetch Logic Branch Prediction **Memory Queue** Floating-point Register File Integer Register
www-ece.rice.edu/~sarita/Publications/tcca1097.ps

Harnessing User-Level Networking Architectures for.. - Madukkarumukumana, Shah (1998) (Correct) (10 citations)
from multiple work queues to a single **queue. Memory** protection for all VI operations is provided
www.usenix.org/publications/library/proceedings/usenix-nt98/full_papers/madukkarum/madukkarum.pdf

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of premature store prefetches and insufficient **memory queue** sizes. The second part of the paper proposes
of premature store prefetches and insufficient **memory queue** sizes. Our second contribution is a new
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Design Issues for High Performance Active Routers - Wolf, Turner (2000) (Correct) (9 citations)
used for packet classification and one to a **Queue Memory** (QM) used to store packets awaiting processing
Since the packets can be brought in from the **Queue Memory** as needed, then promptly written back out, not
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upper and lower bounds on the maximum per-**queue memory** capacity for a k-queue scheduling algorithm
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The Impact of Exploiting Instruction-Level.. - Pai, Ranganathan.. (1999) (Correct) (4 citations)
Instruction window (reorder buffer) size 64 **Memory queue** size 32 Outstanding branches 8 Functional
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wish to know the expected length of the maximum **memory queue** in such a case. As hardware costs go down, the
at the probability distribution of the maximum **memory queue** length. We derive a recurrence relation for
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to ignore feedback information. The impact of **memory queue** size, feedback threshold value, and bleeding
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Memory Optimization in Single Chip Network Switch Fabrics - David Whelihan Herman (2002) (Correct) (2 citations)
technique for maximizing the e#ectiveness of **queue memory** in a single chip switch. Next, we show
output blocks are grouped together with output **queue memory** and a switch-box unit. These nodes are then
have more than 1 MB per port of output **queue memory**[18]Also, the worst case tra#c at any one
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with a circuit-switched bus. Apart from the **memory queue**, the model contains a delay server
end Figure 1. SPMD code of the sample program **memory queue** and the delay server are respectively Dm =
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like the KSR or the Cray Y-MP. Priority **queue Memory** Space Computing activity Figure 1: Typical
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A Case for Staged Database Systems - Harizopoulos, Ailamaki (2003) (Correct) (1 citation)
where the scheduling objective is to minimize **queue memory** and response times, while providing results at
www-db.cs.wisc.edu/cidr/program/p3.pdf

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copies each entity state block into a circular **memory queue**. COMPOSE implements a simple Moving Time
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This problem can be overcome with a shared-**memory queue** and a pair of hardware and software semaphores
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Understanding The Effects of Wrong-Path Memory - References On Processor (2004) (Correct)
servicing older instructions' requests earlier. **Memory Queue** and L2 Fill Queue are modeled as FIFO queues.
one from the Bus Request Queue and one from the **Memory Queue**. Processor frequency is four times the bus
execution can only a#ect D-Cache Bus Request Queue **Memory Queue** DRAM Memory Banks I-Cache I-Cache
www.cs.utah.edu/wmpi2004/papers/paper-139.pdf

System-On-Chip Internet Firewall - John Lockwood Christopher (Correct)
and tail pointers for each list -Track free **memory Queue** Management Enqueue packet -Dequeue
www.mseconference.org/mse_03_archive/mse03_5_Lockwood_SOCFirewall.pdf

Juniper Networks, Inc. 1194 North Mathilda Avenue.. - Part Number Supporting (Correct)
discussions of queue scheduling disciplines, **queue memory** management, host TCP congestion-avoidance
ahead of it. During periods of congestion, the **queue memory** management and queue scheduling disciplines
classes. Generally, you will not use RED as a **queue memory**-management mechanism when supporting the EF
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This can introduce substantial computational and **memory** overheads in processing the data. ffl Data
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have been proposed for such distributed **memory** concurrent computer systems. They include
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Application-Controlled File Caching Policies - Cao, Felten, Li (1994) (Correct) (58 citations)
pages (replacement)Previous work on two-level **memory** management has focused on replacement, largely
ftp.cs.princeton.edu/reports/1994/445.ps.Z

The Zebra Striped Network File System - Hartman, Ousterhout (1993) (Correct) (152 citations)
the performance of a single server, including its **memory** bandwidth and the speed of its processor, network
www.cs.arizona.edu/people/jhh/papers/zebra_tocs.ps

Beyond Depth-First: Improving Tabled Logic Programs through.. - Freire (1996) (Correct) (9 citations)
be efficient in terms of time and space for in-**memory** queries. 16] showed that, compared to Prolog,
www.cs.sunysb.edu/~tswift/webpapers/plilp-96.ps.gz

Hardware for Speculative Reduction Parallelization and .. - Zhang, Rauchwerger.. (1999) (Correct) (2 citations)
in an effective manner on Distributed Shared-**Memory** (DSM) multiprocessors, some important codes would
www-apache.imag.fr/manifestations/PCIA/paper6.ps

Performance Comparison Of Video Transport Over ATM.. - Hossain, Kang, Horst (Correct)
or MPEG-1)mmaps the video file to the user **memory**, then gradually reads an integral number of
writes a chain of BTE (Block Transfer Engine) **descriptors** in the main **memory** (MM) of machine A (Figure
memory (MM) of machine A (Figure 7)Each BTE **descriptor** is responsible for 4 KBytes (max) of data (for
berserk.visi.uiuc.edu/people/ashfaq/ieee.mm97.ps

JaDE: Access Control in a Java-Based Object Database - Jones Winslett (1995) (Correct) (1 citation)
that eliminates the possibility of overwriting **memory** and corrupting data [Cor95a]The Java compiler
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Tiling with Limited Resources - Calland, Dongarra, Robert (1997) (Correct) (4 citations)
with pipelined arithmetic units and a multi-level **memory** hierarchy (this is illustrated by recasting
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Fault Tolerant Matrix Operations for Networks of Workstations.. - Kim, Plank (1997) (Correct) (6 citations)
and rollback recovery using processor and **memory** redundancy with any reliance on disk. Its
www.netlib.org/utk/papers/hpc97/hpc97.ps

An Architecture for Optimal All-to-All Personalized.. - Hinrichs, Kosak.. (1994) (Correct) (38 citations)
four messages simultaneously, i.e. have twice the **memory** bandwidth as incoming network bandwidth. Horie
www.cs.cmu.edu/afs/cs.cmu.edu/project/iwarp/archive/iWarp-papers/cmu-cs-94-140-all-to-all.ps

Tools for Building Asynchronous Servers to Support Speech and.. - Arons (1992) (Correct) (6 citations)
the server itself, such as number of clients, **memory** usage, etc. Each service is provided on a
information from sockets, additional file **descriptors** can be registered with the SM. This allows
2 I.e.all arguments are call by value. file **descriptor** that identifies the entity on the other end of
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stories are fundamental constituents of human **memory** and new experiences are interpreted in terms of
Each inspirational story is indexed with three **descriptors**: Commandments"Nouns" and "Verbs"The
about the point being made by that story. The **descriptor** "Commandments" is weighted more heavily because
gn.www.media.mit.edu/groups/gn/publications/marina_icls_96.ps

A Polygonal Approximation to Direct Scalar Volume Rendering - Shirley, Tuchman (1990) (Correct)
(86 citations)
volume rendering, but is faster and has smaller **memory** requirements. The method is best suited for
data. CR Categories and Subject **Descriptors**: I.3.0 [Computer Graphics]General I.3.5
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model. Our experimental platform is a distributed **memory** machine called MANNA [6]An interesting feature
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Building Multithreaded Architectures with Off-the-Shelf.. - Hum, al. (1994) (Correct) (15 citations)
as the basis of program execution, and the MTA **memory** hierarchy. Section 3 gives more details about the
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Automated Verification of Concurrent Linked - Lists With Counters (Correct)
" denotes that the verifier ran out of **memory**. Number of Queue Stack TwoLockQueue Processes HC integer variables and heap variables such as **head** 6= null !numItems ?0. The presented technique Linked Lists 3 module main(heap -next **head**, **tail**, add, get, newHead boolean mutex integer
www.cs.ucsb.edu/~bultan/publications/sas02.ps

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"consume: buffer empty" endl return-1 c =cb[**head**]length-incr(**head**)increment with produce: buffer full" endl return-1 cb[**tail**] c lengthincr(**tail**)return 0 OOP3-36 endl return-1 cb[**tail**] c lengthincr(**tail**)return 0 OOP3-36 ICM private: int
symbolicnet.mcs.kent.edu/~pwang/oop/slide3-2D.pdf

Enhanced Schema-Based Transformations for Logic Programs.. - Vasconcelos, Fuchs (1995) (Correct) (2 citations)
the following schema schema_A(1schema_A(**Head**|**Tail**]2pre_process(3Head,4 following schema schema_A(1schema_A(**Head**|**Tail**]2pre_process(3Head,4 pre_process(3Head,4schema_A(**Tail**,5post_process(6Head,7where the
ftp.ifi.unizh.ch/pub/techreports/TR-95/ifi-95.16.ps.gz

Theory and Simulation of the Electron Cloud Instability - Rumolo And Zimmermann (Correct) (2 citations)
instabilities on a circulating beam through a **head-tail** coupling mechanism. The oscillation frequency instabilities on a circulating beam through a **head-tail** coupling mechanism. The oscillation frequency of in plasma physics. In this case, the **head** and the **tail** motions of a single bunch are coupled by the
wwwslap.cern.ch/collective/electron-cloud/chamonix11/charn_GR.pdf

Transverse Performance Of The Proton Beam Delivered - The Cern Ps (Correct)
Furthermore, collective effects, such as high-order **head-tail** instabilities induced by the resistive-wall collective effects, such as high-order **head-tail** instabilities induced by the resistive-wall horizontal coupled-bunch instabilities having **head-tail** mode number m =5and coupledbunch mode numbern
accelconf.web.cern.ch/accelconf/e00/PAPERS/MOP6B06.pdf

Single Bunch Collective Effects in the ALS - Byrd Corlett And (Correct)
energy spread increase, HOM loss measurements, **head-tail** damping rates, current dependent tune shifts, energy spread increase, HOM loss measurements, **head-tail** damping rates, current dependent tune shifts, and betatron tune shift vs. bunch current and the **head-tail** damping rate vs. bunch current and chromaticity.
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Information Theory and Neural Network Learning Algorithms - Plumbley (1992) (Correct) (2 citations)
. If one of the outcomes has probability P(w) w **head tail** 1.0 P(w|X=**head**) w **head tail** 1.0 (a) b) one of the outcomes has probability P(w) w **head tail** 1.0 P(w|X=**head**) w **head tail** 1.0 (a) b) Figure P(w) w **head tail** 1.0 P(w|X=**head**) w **head tail** 1.0 (a) b) Figure 1. Probabilities of coin
www.eee.kcl.ac.uk/~mdp/papers/1992/irish92.ps.gz

Separate Compilation for - Matthias Blume Department (Correct)
(define-type streams-sig (signature (nil **head tail** stream-cons) constant nil any) constant (define-type streams-sig (signature (nil **head tail** stream-cons) constant nil any) constant **head** any) constant **head** (proc any -any)constant **tail** (proc any -any)use scheme-sig) define-syntax
www.cs.Princeton.edu/~blume/modules.ps

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1 Artificial Life 2(4)377-416, 1995. 2 **Tail Head Tail** Fiber Figure 1: the pathway of T4
Artificial Life 2(4)377-416, 1995. 2 **Tail Head Tail** Fiber Figure 1: the pathway of T4 bacteriophage shows formation of a subassembly a **head** and a **tail** form a **head-tail** subassembly, and this subassembly
www-personal.engin.umich.edu/~kazu/papers/alifej-95b.pdf

Auburn: A Kit for Benchmarking Functional Data Structures - Graeme Moss And (1997) (Correct) (1 citation)
[Oka96a]module Queue (Queue,empty,snoc,**tail**,**head**,isEmpty) where empty :Queue a snoc :Queue a - from [Oka96a]module Queue (Queue,empty,snoc,**tail**,**head**,isEmpty) where empty :Queue a snoc :Queue empty :Queue a snoc :Queue a -a -Queue a **tail** :Queue a -Queue a **head** :Queue a -a isEmpty
ftp.cs.york.ac.uk/pub/colin/ifl97m.ps.gz

Slac-Pub-95-6965 - August Transverse Multibunch (Correct)
mechanism for the rigid (m =0) motion to drive the **head-tail** (m =1) motion, or vice-versa (only for the rigid (m =0) motion to drive the **head-tail** (m =1) motion, or vice-versa (only considering **head** of the bunch sees no wakefield, whereas the **tail** of the bunch sees the wakefield of the entire
jsberg.home.cern.ch/jsberg/docs/ps/95-6965.ps.gz

Coalgebraic Modal Logic of Finite Rank - Kurz, Pattinson (Correct)
a set D consider TX =DX. Given a coalgebra **head**, **tail**# C DC the behaviour of an element c D consider TX =DX. Given a coalgebra **head**, **tail**# C DC the behaviour of an element c C is element c C is the innite list **head**(c)**head**(**tail**(c)**head**(**tail**(**tail**(c)Accordingly, the
www.cwi.nl/~kurz/SEN-R0222/SEN-R0222.ps.gz

Static Typing for Dynamic Messages - Nishimura (1998) (Correct) (8 citations)
method map(msglst) case msglst of [j **head**:**tail**)self/**head**)self/map(**tail**)end where map(msglst) case msglst of [j **head**:**tail**)self/**head**)self/map(**tail**)end where [of [j **head**:**tail**)self/**head**)self/map(**tail**)end where [stands for an empty list,
ftp.kurims.kyoto-u.ac.jp/pub/paper/member/nisimura/dmesg-popl98-a4.ps.gz

Definability, Canonical Models, Compactness for Finitary.. - Kurz (2002) (Correct)
behaviour of an element a 2 A is the innite list (**head**(a)**head**(**tail**(a)**head**(**tail**(**tail**(a) D consider TX =DX. Given a coalgebra hhead **taili** :A !DA the (complete) behaviour of an element an element a 2 A is the innite list (**head**(a)**head**(**tail**(a)**head**(**tail**(**tail**(a)Accordingly, the
www.pst.informatik.uni-muenchen.de/~pattinso/Publications/cmcs2002.ps.gz

Observation Of Vertical Beam Blow-Up In Kekb Low Energy Ring - Fukuma Akai Akasaka (Correct)
the electron cloud appears as either weak or strong **head-tail** instability. A beam-size blow-up will be cloud appears as either weak or strong **head-tail** instability. A beam-size blow-up will be observed blow-up will be observed as a result of the **head-tail** oscillation of the instability. In this model the
wwwslap.cern.ch/collective/electron-cloud/kekb/WEP5A12.pdf

WebGrid: Knowledge Modeling and Inference through the World.. - Brian Gaines And (1996) (Correct) (1 citation)
mm mm mm mm errors sign wind -**tail head head tail tail head tail head** mag -out
mm mm mm mm mm mm errors sign wind -**tail head head tail tail head tail head** mag -
mm errors sign wind -**tail head head tail tail head tail head** mag -out light med
repgrid.com/reports/KBS/KMD/KMD.pdf

An Interconnect Energy Model Considering Coupling Effects - Uchino, Cong (Correct) (2 citations)
where A vi 1 (A vi 1) if node v is the **head** (**tail**) 1 of edge i, and A vi 0 otherwise.
A vi 1 (A vi 1) if node v is the **head** (**tail**) 1 of edge i, and A vi 0 otherwise. The
where i j (the j-th element of vec- 1 The **head** (**tail**) of an edge is the node to (from) which the edge
ballade.cs.ucla.edu/~cong/papers/34_21.pdf

RPT: A Low Overhead Single-End Probing Tool - For Detecting Network (2003) (Correct)
destination. Traceroute sets the TTL in the IP **head**er to trigger responses from the routers along the packet is linearly incremented from the **head/tail** packet, and the **head/tail** packet has TTL value 1. incremented from the **head/tail** packet, and the **head/tail** packet has TTL value 1. The train in Figure 1 can
reports-archive.adm.cs.cmu.edu/anon/2003/CMU-CS-03-218.ps

Study Of Fast Ion Instability At Kekb Electron Ring - Ohnishi Fukuma Kikutani (Correct)

bunches passing through the BOR were stored in the **memory** turn by turn up to 4096 turns which corresponds in a bunch train. The bunch oscillations in the **head** of the bunch train is very small in comparison bunch train is very small in comparison with the **tail** as shown in Fig. 2(d)This behavior may show ions
accelconf.web.cern.ch/AccelConf/e00/PAPERS/WEP1A07.pdf

ParaDOS: A Parameterized, Parallel and Distributed Operational.. - Smith (1998) (Correct)
usually takes the form of a common, shared **memory** space accessible by a PDS's executing processes, (test3) Value: 42 60 e (cdr c) d)Case 5: if **head**(C) and **head**(**tail**(S)is a predef. function f e (cdr c) d)Case 5: if **head**(C) and **head**(**tail**(S)is a predef. function f (and (eval? car c)
www.cs.ucf.edu/~mlsmith/tr9905.pdf

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SL Note 2001-043 (MD) - Measurements Of Sps (2001) (Correct)
of SPS SingleBunch Coherent Tune Shifts and **Head-Tail** Growth Rates in the Year 2001 H. Burkhardt, of SPS SingleBunch Coherent Tune Shifts and **Head-Tail** Growth Rates in the Year 2001 H. Burkhardt, G. measurements based on coherent tune shift and **head-tail** growth and decay rates is based on Sacherer [7]
sl.web.cern.ch/SL/Publications/md2001-043.pdf

Practical Issues Of 2-D Parallel Finite Element Analysis - Michelle Hribar (Correct)
appropriate, the impact on the subdomain size, the **memory** requirements versus the actual **memory** of the of 480 bytes of data and 32 bytes for the **header** [8]3.2 Communication Parameters The ff, fi,
ece.nwu.edu/pub/CELERO/picpp94.ps.gz

Using PVM 3.0 to Run Grand Challenge Applications on.. - Dongarra, Geist.. (1992) (Correct)
on the nodes of several different distributed **memory** multiprocessors as though they constitute one [K s K r (rh rz)q where h is the pressure **head**, t is time, K s is the saturated hydraulic
ftp.netlib.org/ncwn/siam93-pvmgc.ps

Customized Dynamic Load Balancing for a Network of.. - Zaki, Li, Parthasarathy (1995) (Correct) (19 citations)
scalability in terms of computation power and **memory** size. With the rapid advances in new high speed
ftp.cs.rochester.edu/pub/papers/systems/95.tr602.Customized_dynamic_load_balancing.ps.gz

On the Utility of Threads for Data Parallel Programming - Fahringer, Haines, Mehrotra (1995) (Correct) (4 citations)
a lightweight thread package for distributed **memory** multiprocessors, called Chant [5]to encode 2
ftp.icase.edu/pub/techreports/95/95-35.ps.Z

Automatic Data Decomposition for Message-Passing Machines - Damian-Iordache, Pemmaraju (1997) (Correct) (1 citation)
data distributions)1 Introduction Distributed-**memory** message-passing parallel computers are becoming
ftp.cs.uiowa.edu/pub/sriram/graphs/IcpcTr.ps.gz

Thread Migration and its Applications in Distributed.. - Itzkovitz, Schuster, .. (1996) (Correct) (37 citations)
and W. Zwaenepoel. Treadmarks: Distributed Shared **Memory** on Standard Workstations and Operating Systems.
casaturn.kaist.ac.kr/~sikang/course/CS614/ISW96.ps.gz

Mesh Component Design and Software Integration within SUMAA3d - Freitag, Jones, Plassmann (Correct)
x Abstract The requirements of distributed-**memory** applications that use mesh management software
info.mcs.anl.gov/pub/tech_reports/reports/P726.ps.Z

Foundation for - Research And (Correct)
exploited, while still guaranteeing a low level of **memory** contention, so that performance does not suffer
ftp.ics.forth.gr/lydia/Publications/Mavronic_pubi1.ps.gz

Some MPEG Decoding Functions on Spert An Example for Assembly.. - Formella (1994) (Correct) (1 citation)
merge) Spert is a board equipped with one T0 and **memory** which can be used in a workstation. In the
ftp.icsi.berkeley.edu/pub/techreports/1994/tr-94-027.ps.gz

Using Write Protected Data Structures To Improve Software Fault.. - Sullivan (1991) (Correct) (10 citations)
a record it intends to update into unprotected **memory** and updates the copy. At the end of transaction, call. While the page is unprotected, the page **header** can be manipulated directly (for updates and
s2k-ftp.cs.berkeley.edu:8000/postgres/papers/ERL-M91-56.ps.Z

Parallel Solutions to Geometric Problems in the Scan Model.. - Blelloch, Little (1994) (Correct) (7 citations)
access machines) attached to a single shared **memory**. Processors communicate through the shared segment. The segments will never overlap and the **head** is easy to identify (a pointer to SAMPLEUP(v)
www.cs.cmu.edu/afs/cs.cmu.edu/project/scandal/public/papers/jcss-geom.ps.gz

User-Level DMA without Operating System Kernel Modification - Markatos, Katevenis (1997) (Correct) (7 citations)
Abstract Direct **Memory** Access (DMA) is frequently used to transfer data
www.ccsf.caltech.edu/~markatos/avg/papers/1997.HPCA97.user_level_dma.ps.gz

An Effective Design System for Dynamically Reconfigurable.. - Sriram Govindarajan (Correct) (2 citations)
(rc) that consists of a multi-fpga board with **memory** banks and interconnection fabric, is being widely
www.ece.uc.edu/~sriram/papers/fccm98.ps

Fractional Brownian Motion and the Markov Property - Carmona, Coutin (1998) (Correct) (2 citations)
Brownian motion belongs to a class of long **memory** Gaussian processes that can be represented as
www-sv.cict.fr/lsp/Carmona/fbmarkov.ps

Coordinated Checkpointing-Rollback Error Recovery for.. - Janakiraman, Tamir (1994) (Correct) (32 citations)
Error Recovery for Distributed Shared **Memory** Multicomputers G. Janakiraman and Yuval Tamir
ftp.cs.ucla.edu/tech-report/94-reports/940027.ps.Z

Algorithmic Redistribution Methods for Block Cyclic.. - Petitet, Dongarra (1998) (Correct) (9 citations)
of the hardware resources. In a distributed-**memory** environment, load balance is the essential
netlib.uow.edu.au/lapack/lawns/lawn133.ps

Matching Micro-Kernels to Modern Applications using.. - Ciaran Bryce (1995) (Correct) (3 citations)
to Modern Applications using Fine-Grained **Memory** Protection Ciaran Bryce &Gilles Muller
discussed in section 5. Protected modules contain a **header** code which is invoked on each PPC this code is our approach allows certain system functions to be **tailored** to a particular application's needs we are
www.fcul.research.ec.org/broadcast/trs/./papers/97.ps

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SPRINT: A Scalable Parallel Classifier for Data Mining - Shafer, Agrawal, Mehta (1996) (Correct) (130 citations)
all the time. Since the size of this in-**memory data structure** grows in direct proportion to the number
www.almaden.ibm.com/cs/people/ragrawal/papers/vldb96_sprint.ps

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Fine-grain Access Control for Distributed Shared Memory - Schoinas (1994) (Correct) (108 citations)
The code in a software lookup checks a main-**memory data structure** to determine the state of a block before
www.ece.purdue.edu/~babak/papers/asplos-vi.ps

On Optimal Multiversion Access Structures - Becker, Gschwind, Ohler.. (1993) (Correct) (26 citations)
More precisely, any single version main **memory data structure** in a very general class, based on
ftp.inf.ethz.ch/doc/papers/ti/grpw/ssd93.ps.gz

High-dimensional Similarity Joins - Shim, Srikant, Agrawal (1997) (Correct) (23 citations)
called the ffl-kdB tree. This is a main-**memory data structure** optimized for performing similarity
www.almaden.ibm.com/cs/quest/papers/de97_ekdb.ps

Cryptfs: A Stackable Vnode Level Encryption File System - Zadok, Badulescu, Shender (1998) (Correct) (15 citations)
privileges, Cryptfs maintains keys in an in-**memory data structure** that associates keys not with UIDs alone
ftp.cs.columbia.edu/reports/reports-1998/cucs-021-98.ps.gz

Design and Performance Evaluation of a Multithreaded.. - Govindarajan.. (1995) (Correct) (15 citations)
S.U. F.U. I.I.R I.I.R I.R I.R Router **Memory Data Structure** To other PEs .Queue Score Board
www-acaps.cs.mcgill.ca/~govind/HPCA-95.ps.gz

Scalable Mining for Classification Rules in Relational.. - Wang, Iyer, Vitter (1998) (Correct) (6 citations)
classifiers [21, 25] need an in-**memory data structure** of size O(N)where N is the size of the
www.cs.duke.edu/~jsv/Papers/WIV98.classification.ps.gz

The String B-Tree: A New Data Structure for String Search in .. - Ferragina, Grossi (1998) (Correct) (4 citations)
memory. As far as traditional external-**memory data structures** are concerned, inverted files [39]
www.math.tau.ac.il/~matias/courses/papers/string_btree.ps

Toward a Machine Assisted Software Performance Diagnosis.. - Mathur, Abrams (1993) (Correct) (2 citations)
strong hypothesis defines a code segment or **memory data structure** X as a primary performance bottleneck and
www.cs.vt.edu/~chitra/docs/93tr-12.ps

Building Common Lisp Applications with Reasonable Performance - Boreczky, Rowe (1993) (Correct) (1 citation)
ad hoc queries to a database. The main **memory data structure** for the facility floorplan including
www.unfortu.net/pub/db/picasso/Picasso-papers/LUV93.ps.Z

A User's Manual and Guide to an SDM Simulator on a Connection .. - Marshall, Meeden (1989) (Correct)
comprise the entire sparse distributed **memory data structure**. 2.2 Read and Write Operations To
www.cs.swarthmore.edu/~meeden/meeden.sdm.manual.ps.Z

Efficient Searching with Linear Constraints (Extended .. - Agarwal, Arge.. (Correct)
a set S of points in R d into an external **memory data structure** that efficiently supports
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called the ffl-kd tree. This is a main-**memory data structure** optimized for performing proximity joins.
www.almaden.ibm.com/cs/people/srikant/papers/de97_rj.ps

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This is achieved by using an auxiliary main **memory data structure** called the active border which requires
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A Compilation Approach for Fortran 90D/HPF Compilers on.. - Zeki Bozkus (1993) (Correct) (8 citations)
not generate code for scheduling but it passes a **pointer** to the already existing schedule. Furthermore, for Fortran 90D/HPF Compilers on Distributed **Memory** MIMD Computers Zeki Bozkus, Alok Choudhary y prone because the user must perform the task of **data** distribution and communication for non-local **data**
ftp.npac.syr.edu/pub/docs/sccs/papers/ps/0450/sccs-0499.ps.Z

Space Efficient Parallel Buddy Memory Management - Johnson, Davis (1992) (Correct) (5 citations)
satisfy the request by allocating the block at the **head** of the level i free list, if possible. If there is into a single word)Free blocks also contain two **pointers** to maintain a doubly linked list. The buddy requests for **memory** blocks of size i. 3. **Queue**: A **queue** of blocked allocate requests. 4. Lock: A
ftp.cis.ufl.edu/cis/tech-reports/tr92/tr92-008.ps

Providing Real-Time Response, State Recency and Temporal.. - Datta, Viguier (1996) (Correct)
install U(D j)However, when U(D i)reaches the **head** of the update **queue**, it would be discarded (i.e. of sensor **data** include link utilization and node **queue** lengths from the network management domain, stock any such assumption. Additionally, 3] considers a **memory** resident **data**base while we consider a disk
loochi.bpa.arizona.edu/pub/publications/sigmod96.ps.gz

Case Study: Observing a Volume Rendered Fetus.. - State, Chen.. (1994) (Correct) (6 citations)
Augmented reality systems with see-through **head**mounted displays have been used primarily for as overlays for wiring guides or informational **pointers**, will be able to get by, but applications with 1 Introduction Interpreting 3D radiological **data** is difficult for nonexperts because understanding
www.cs.unc.edu/Research/stc/pubs/volume_rendered_fetus.ps.gz

Databases for Active, Rapidly, Changing data Systems (ARCS) and.. - Datta (1996) (Correct) (1 citation)
the sensor **data** may include variables such as node **queue** lengths, retransmission rates, link status and That Is Used By The Procedures. The St Array Is A **Memory** Resident Array Of Dimension Numsensor Where The
Databases for Active, Rapidly, Changing **data** Systems
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Principal Component Analysis on Vector Computers - Martin, Blanco, Heras.. (1995) (Correct) (1 citation)
are too short .ffl Loop fusion. ffl Optimize **memory** access, exploiting **data** locality. ffl Unroll in as a statistical tool for reducing multivariate **data** encountered in applied statistical research to a purpose of analysing covariance and correlation **structures**. Since then, it has become increasingly popular
ftp.ac.uma.es/pub/reports/1995/UMA-DAC-95-21.ps.gz

An Introduction to Disk Drive Modeling - Ruemmler, Wilkes (1994) (Correct) (258 citations)

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Patterns in Random Binary Search Trees - Flajolet, Gourdon, Martinez (1996) (Correct) (8 citations)
on short subfiles. As a consequence, various **pointer** saving strategies for maintaining trees obeying also applies to heap-ordered trees for priority **queue** maintenance [40, 43]to tree representations of "paging"where one has a two-level hierarchical **memory** structure: the index resides in main **memory** and
pauillac.inria.fr/algo/flajolet/Publications/RR2997.ps.gz

Cache Performance of Fast-Allocating Programs - Marcelo Goncalves (1995) (Correct) (4 citations)
the allocation space. We only need to keep two **pointers**, one to the next free address, the allocation 1 Introduction With the gap between CPU and **memory** speed widening, good cache performance is that. It is therefore important to understand the **memory** behavior of programs, so that computer architects
www.cs.princeton.edu/~mjrg/fpca95.ps.Z

Reasoning about Aliasing - Utting (1997) (Correct) (13 citations)
LList schema defines the whole linked list, with a **head** and tail **pointer** and a local store (the sequence Email: marku@cs.waikato.ac.nz Keywords: Aliasing, **Pointers**, Object-Orientation, Refinement Calculus. requests to: Mark Utting Mark Utting A simple **Queue** abstract data type (ADT) is used to illustrate
www.cs.waikato.ac.nz/~marku/papers/aliasing.ps.gz

Cognitive Walkthrough - Usability Evaluation Materials - Lavery, Cockton (1997) (Correct)
Figure 2)He selects the text by moving the mouse **pointer** to the beginning of the text, holds the mouse
www.dcs.gla.ac.uk/publications/reports/1997-20.ps

The LooPo scanner and parser - Frank Schuler (1995) (Correct) (1 citation)
The definition Two types are defined. Entry is a **pointer** to a node object and SymbolTable is an object *root: root entry of the binary tree *lexemes: **memory** area for the lexem strings of size StrMax * lookahead to the next token *coef: cache **memory** for index variable coefficients *c0: cache
brahms.fmi.uni-passau.de/ci/loopo/doc/schuler-p.ps.gz

Don't Stop the BIBOP: Flexible and Efficient Storage.. - Dybvig, Eby, Bruggeman (1994) (Correct) (4 citations)
system, objects are reachable only through their **head**ers. By keeping large objects in a separate large system's hybrid type representation employs typed **pointers** and typed objects for tagging individual in the segment table, and places the object on a **queue** for later sweeping (if necessary)For newly
ftp.cs.indiana.edu/pub/techreports/TR400.ps.Z

PFSLib - Using Intel's Parallel I/O Interface on Coupled.. - Röder, Lamberts, Bode (Correct)
M UNIX provides each process with its own file **pointer** and it is the programmer's responsibility to carries out the file access. Unix IPC shared **memory** is used for the data transfer between client and standard message passing interface for distributed **memory** concurrent computers. Parallel Computing,
ftp.irisa.fr/local/CMPI/EISUG95/Christian.Roeder-paper.ps

Recycling in Gardens: Efficient Memory Management for a Parallel .. - Siu Yuen (Correct)
tasks' heaps. These object references (global **pointers**) support a very efficient form of remote method Recycling in Gardens: Efficient **Memory** Management for a Parallel System Siu Yuen Chan, and tasks. This paper presents the Gardens **memory** management model, its implementation and some
sky.fit.qut.edu.au/~proe/papers/PART98.ps.gz

Characterizing the Performance of Algorithms for Lock-free Objects - Johnson (Correct)
defined by an atomic snapshot of the value of the **head pointer**, the tail **pointer**, and the next-record implementation. An object is represented by a **pointer** to its current instantiation. A process performs 37]AVL trees [15]B-trees [8, 53]priority **queues** [12, 46, 30] and so on. Shasha and Goodman [54]
ftp.cis.ufl.edu/pub/tech-reports/tr93/tr93-021.ps.gz

Adding Persistence to the Oberon-System - Knasmüller (1996) (Correct)
and Print (to print the list)Each list has a **head**er containing the field font, which determines the
Will Be Shortly Outlined Below. Type Object =**Pointer** To Objectdesc Objectdesc =Record Objectfields
heap, while transient objects are in the transient **memory**. Transient and persistent objects can access each
ftp.ssw.uni-linz.ac.at/pub/Papers/PersOberon.ps.Z

Service Combinators for Web Computing - Cardelli, Davies (1997) (Correct) (22 citations)
to mind is the lack of referential integrity: a **pointer** (URL 1 on the Web does not always denote the
of the fundamental properties of traditional (in-**memory**, or localarea) object systems. The first problem
www.cs.cmu.edu/afs/cs/user/rowan/www/papers/service.ps

C Threads - Coopers, Draves (1990) (Correct)
Package 3.1. cthreads.h include cthreads.h The **head**er file cthreads.h defines the C threads interface.
indicates that the mutex_t type is defined as a **pointer** to a referent type struct mutex which may itself
are to have one mutex protecting all shared **memory**, and to have one mutex for every byte of shared
ftp.cs.cuhk.hk/pub/mach3/doc/techreports/threads.ps

Efficient Translation of External Input in a Dynamically Typed.. - Paige (1994) (Correct) (2 citations)
Our algorithms are based on a sequential **pointer** RAM model of computation [4, 7]which accesses
in the input and the sentinel are stored in **memory** within an initial universe U of data items each
ftp.diku.dk/diku/semantics/papers/D-226.ps.gz

Using the Co-existence Approach to Achieve Combined.. - Ananthanarayanan.. (1993) (Correct) (4 citations)
to their data modeling power, OOSs offer fast **pointer**-based traversal of objects at or near **memory**
and their ability to perform data operations at **memory** speeds. The modeling power of OOSs stems from a
fast **pointer**-based traversal of objects at or near **memory** speed because they not only bring the data into
www.cc.gatech.edu/computing/Database/students/vibby/papers/smrc-93.ps.Z

Evaluation Of A Stack Decoder On A Japanese Newspaper Dictation .. - Mike Schuster (1996) (Correct)
its LM probability and backoff probability, and a **pointer** to the beginning of the list of extension word
on a 300 Mhz Pentium II. Using a disk-based LM the **memory** usage could be optimized to 4 MB in total. 1. A
Because They Made To A Large Extent A Time- And **Memory**efficient Search Possible. 1.1. N-Gram Module A
isw3.aist-nara.ac.jp/IS/Shikano-lab/staff/1996/mike-s/papers/asj98.2.ps.gz

A Vision-Guided, Semi-Autonomous System Applied to a.. - Seelinger Robinson (Correct)
graphical interface, several cameras, a laser **pointer** mounted on a two-axis pan/tilt unit, and a six
www.nd.edu/~mseeling/papers/spie97.ps

Parallel Algorithms - Blelloch, Maggs (1996) (Correct) (2 citations)
balancing, and routing algorithms. 3. Parallel **Pointer** Manipulations. Many of the traditional
the PRAM model, a set of processors share a single **memory** system. In a single unit of time, each processor
processor can perform an arithmetic, logical, or **memory** access operation. This model has often been
www.cs.cmu.edu/afs/cs.cmu.edu/project/phrensy/pub/papers/BleilochM96.ps

Graphs in Compilation - Claessen (1997) (Correct)
by a node in a graph. A use of that variable is a **pointer** to that node. The node will be overwritten by an
to use `real' **pointers**, as in addresses in the **memory** of a computer. Haskell also offers a way to do
ftp.cs.chalmers.se/pub/users/koen/Papers/abstract.ps

Meta-level Architecture for Extendable C++ - Ishikawa (1994) (Correct) (7 citations)
: 5 2.4.2 Global **Pointer**
have been introduced to access the remote **memory** area in Split-C[3]EM-C[16]and CC2]To
pointer that makes it possible to access remote **memory** in a distributed **memory** parallel machine
jisp.cs.nyu.edu/RWC/rwcp/people/yk/rwcp-doc/papers/1994/tr94024.ps.gz

PFSLib - A Parallel File System for Workstation Clusters - Ludwig, Lamberts (1995) (Correct)
M UNIX provides each process with its own file **pointer** and it is the programmer's responsibility to
carries out the file access. Unix IPC shared **memory** is used for the data transfer between client and
standard message passing interface for distributed **memory** concurrent computers. Parallel Computing,
www.ntua.gr/parallel/libraries/communication/pfslib/PAPER/PaCT.ps.gz

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Applicant: ADVANCED MICRO DEVICES INC (US)
EC:
IPC: H04L12/50
Publication info: **US6885666** - 2005-04-26

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Inventor: HE YAN JIAO (CN)
Applicant: FIBERHOME TELECOMM TECHNOLOGIE (CN)
EC:
IPC: H04L12/28; H04L12/24; (+1)
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IPC: H04L12/54
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IPC: G06F12/08
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Applicant: YINGHUADA SHANGHAI ELECTRONICS (CN)
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IPC: G06F12/00; G06F9/38
Publication info: **CN1536489** - 2004-10-13

6 **Method and system for controlling memory accesses to memory modules having a memory hub architecture**
Inventor: JEDDELOH JOSEPH M (US); LEE TERRY R (US)
Applicant:
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Publication info: **US2005066137** - 2005-03-24

7 **Fault tolerant mutual exclusion locks for shared memory systems**
Inventor: MICHEAL MAGED M (US); KIM YONG-JIK (US)
Applicant: IBM (US)
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8 **Dynamic buffer memory management ATM switching arrangement and switching method thereof**
Inventor: ZHANG YAOWEN ZHOU (CN)
Applicant: HUAWEI TECH CO LTD (CN)
EC:
IPC: H04L12/40; H04L12/26; (+2)
Publication info: **CN1522011** - 2004-08-18

9 **Temporary storage of memory line while waiting for cache eviction**
Inventor: LOVETT THOMAS D (US); MICHAEL MAGED M (US); (+2)
Applicant:
EC:
IPC: G06F15/167

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10 **Method and apparatus for maintaining netflow statistics using an associative memory to identify and maintain netflows**

Inventor: OREN EYAL (IL); BELZ DAVID E (IL); (+1) Applicant: CISCO TECH IND (US)

EC: IPC: G06F12/00

Publication info: **US6871265** - 2005-03-22

RESULT LIST
Approximately **587** results found in the Worldwide database for:
memory in the title AND **queue** in the title or abstract
Only the first **500** results are displayed.
(Results are sorted by date of upload in database)

31 **DIRECT MEMORY ACCESS CONTROLLER SYSTEM**
Inventor: CLAYTON SHAWN ADAM; FORTIN BRIAN MARK; (+2) Applicant: EMULEX CORP (US)
EC: IPC: G06F13/24; G06F9/48; (+5)
Publication info: **WO2004061687** - 2004-07-22

32 **READ-WRITE SWITCHING METHOD FOR A MEMORY CONTROLLER**
Inventor: CHRISTENSON BRUCE Applicant: INTEL CORP (US)
EC: IPC: G06F12/00
Publication info: **WO2004061672** - 2004-07-22

33 **Method and apparatus for fetching instructions from the memory subsystem of a mixed architecture processor into a hardware emulation engine**
Inventor: DUA ANUJ (US); MCCORMICK JAMES E (US); (+5) Applicant:
EC: G06F9/318T; G06F9/38F; (+1) IPC: G06F9/30
Publication info: **US2004107335** - 2004-06-03

34 **Method and apparatus for high throughput short packet transfers with minimum memory footprint**
Inventor: LEETE BRIAN A (US) Applicant:
EC: IPC: G06F3/00
Publication info: **US2004093441** - 2004-05-13

35 **Method and apparatus for deadlock prevention with distributed arbitration**
Inventor: MCALLISTER CURTIS R (US) Applicant:
EC: G06F12/08B4P IPC: G06F13/14; G06F13/38
Publication info: **US2004083321** - 2004-04-29

36 **APPARATUS, METHOD AND SYSTEM FOR REDUCING LATENCY OF MEMORY DEVICES**
Inventor: CHAUDHARI SUNIL; VINNAKOTA BAPIRAJU Applicant: INTEL CORP (US)
EC: G06F13/16 IPC: G06F12/00
Publication info: **WO2004031959** - 2004-04-15

37 **NETWORK INTERFACE AND PROTOCOL**
Inventor: POPE STEVEN LESLIE (GB); ROBERTS DEREK EDWARD (GB); (+2) Applicant: LEVEL 5 NETWORKS LTD (GB); POPE STEVEN LESLIE (GB); (+3)
EC: IPC: G06F12/06; G06F12/08
Publication info: **WO2004025477** - 2004-03-25

38 **METHOD FOR OPTIMIZING MEMORY CONTROLLER**
Inventor: CARR JEFFERY D Applicant: IBM
EC: IPC: G06F12/00
Publication info: **JP2004118833** - 2004-04-15

39 **METHOD AND SYSTEM FOR CONTROLLING MEMORY ACCESSES TO MEMORY MODULES HAVING A MEMORY HUB ARCHITECTURE**
Inventor: JEDDELOH JOSEPH M; LEE TERRY R Applicant: MICRON TECHNOLOGY INC (US)
EC: IPC: G06F
Publication info: **WO2004021129** - 2004-03-11

40 **Method and apparatus for providing a packet buffer random access memory**

Inventor: JONES DAVID E (CA)
Applicant: MOSAID TECHNOLOGIES INC (CA)

EC: H04L12/56Q1
IPC: H04L12/54
Publication info: **US2004008714** - 2004-01-15

RESULT LIST
Approximately **541** results found in the Worldwide database for:
memory in the title AND **queue** in the title or abstract
Only the first **500** results are displayed.
(Results are sorted by date of upload in database)

51 **Method for optimizing utilization of a double-data-rate-SDRAM memory system**
Inventor: EMBERLING BRIAN D (US) Applicant:
EC: IPC: G06F12/02
Publication info: **US2004193834** - 2004-09-30

52 **Binding a memory window to a queue pair**
Inventor: GARCIA DAVID J (US); HILLAND JEFFREY R (US); (+3) Applicant:
EC: IPC: G06F12/00; G06F12/14
Publication info: **US2004193825** - 2004-09-30

53 **Method and apparatus for exchanging data between transactional and non-transactional input/output systems in a multi-processing, shared memory environment**
Inventor: LANTEIGNE STEPHEN (CA); LEWIS DAVID (CA) Applicant: NORTEL NETWORKS LTD (CA)
EC: IPC: G06F13/14; G06F13/20; (+1)
Publication info: **US6757756** - 2004-06-29

54 **Memory read/write reordering**
Inventor: SAH SUNEETA (US); KULICK STANLEY S (US); (+3) Applicant:
EC: IPC: G06F12/00
Publication info: **US2003177320** - 2003-09-18

55 **Vector transfer system generating address error exception when vector to be transferred does not start and end on same memory page**
Inventor: ANSARI AHMAD R (US) Applicant: NEC ELECTRONICS INC (US)
EC: G06F9/312; G06F9/38H IPC: G06F15/00
Publication info: **US2003167387** - 2003-09-04

56 **Read-write switching method for a memory controller**
Inventor: CHRISTENSON BRUCE A (US) Applicant: INTEL CORP (US)
EC: IPC: G06F12/00
Publication info: **US2004128428** - 2004-07-01

57 **MULTI-BANK SCHEDULING TO IMPROVE PERFORMANCE ON TREE ACCESS IN DRAM BASED RANDOM ACCESS MEMORY SUBSYSTEM**
Inventor: CALLE MAURICIO; RAMASWAMI RAVI Applicant: AGERE SYSTEMS INC
EC: IPC: G06F12/06; G06F12/02
Publication info: **JP2003208354** - 2003-07-25

58 **DIRECT MEMORY ACCESS DMA TRANSFER BUFFER PROCESSOR**
Inventor: ROACH BRADLEY; DUCKMAN DAVID; (+2) Applicant: EMULEX CORP (US)
EC: IPC: G06F
Publication info: **WO03050655** - 2003-06-19

59 **DDR SDRAM memory controller with multiple dependency request architecture and intelligent requestor interface**
Inventor: NYSTUEN JOHN (US) Applicant:
EC: IPC: G06F12/00
Publication info: **US2004107324** - 2004-06-03

60 SHARED MEMORY CONTROLLER FOR DISPLAY PROCESSOR

Inventor: DEAN JOHN E
Applicant: KONINKL PHILIPS ELECTRONICS NV (NL)

EC: G09G3/20M1; G09G5/393; (+1)
IPC: G06F13/16; G06F3/14

Publication info: **WO03044677** - 2003-05-30